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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,015	RUDECK ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: in line 12, "second oxide layer" should be replaced with --inter-layer insulation--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14 – 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation, "...thereby permitting a trench depth deeper than the self aligned source...". The intended scope of the claim is not known since there are many types of trenches that can be formed in a flash memory device. The type and location of the intended trench is unknown.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 4, 6, 7, 19, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,194,929 to Ohshima et al.

Regarding claim 1, Ohshima et al. teach a semiconductor device (Fig. 5D) comprising:

a substrate (1);

a drain (14,19) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer;

an inter-layer insulation (5) over the first polysilicon layer;

a second polysilicon layer (6) over the inter-layer insulation; and

a phosphorous-doped oxide layer (22; Col. 8, lines 22 – 33 and lines 54 – 57) provided along substantially vertical edges of the first oxide, the first polysilicon layer, the inter-layer insulation and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Regarding claim 2, Ohshima et al. inherently teach a device, wherein the first oxide layer is a tunnel oxide layer, since that is the function of the first oxide layer of the EPROM.

Regarding claim 4, Ohshima et al. teach a semiconductor device, wherein the first polysilicon layer is a floating gate.

Regarding claim 6, Ohshima et al. teach a semiconductor device after re-oxidation (Col. 5, line 68 – Col. 6, line 7) comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) provided along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile formed over surfaces of the semiconductor device having a height and width, since Ohshima et al. teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Regarding claim 7, Ohshima et al. inherently teach a device, wherein the height is a vertical distance from the source to a bottom edge of the first polysilicon layer and the width is a horizontal distance from a side edge of the first polysilicon later to a vertical edge of the tunnel oxide layer, wherein the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide, since Ohshima et al. teach the re-oxidation.

Regarding claim 19, Ohshima et al. teach a semiconductor device comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Regarding claim 20, Ohshima et al. teach a semiconductor device after re-oxidation (Col. 5, line 68 – Col. 6, line 7) comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide

layer and the second polysilicon layer, the phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile having a width defined by a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide [first oxide], wherein the width is less than a re-oxidation profile width without the phosphorus doped oxide layer, since Ohshima et al. teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Regarding claim 21, Ohshima et al. teach a semiconductor device after re-oxidation comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) having a first thickness and stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide

layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile having a width defined by a horizontal distance from a side edge of the first polysilicon layer to a point where said first oxide layer starts to get thicker than said first thickness, and a height defined by a vertical distance from a top surface of said self-aligned source to a bottom edge of said first polysilicon layer, wherein the width is less than a re-oxidation profile width and the height is higher than a re-oxidation profile height without the phosphorus doped oxide layer, since Ohshima et al. teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima et al. in view of US Patent No. 6,732,241 to Riedel.

Ohshima et al. teach a flash memory device comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile formed over surfaces of the semiconductor device having a height and width, since Ohshima et al. teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Ohshima et al. do not teach the flash being used in a computer system comprising:

at least one processor; and

a system bus.

Riedel teaches a computer system including a processor (102) and a system bus (106), wherein the flash memory device is couple to the system bus. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Riedel into the device taught by Ohshima et al., since it is desirable to use the flash device in a functional system.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima et al.

Ohshima et al. do not teach a device, wherein the inter-layer insulation is an oxide nitride oxide (ONO) layer. It is common in the art to use (ONO) layers as the inter-layer insulation film in EEPROM devices. It would have been obvious to one of ordinary skill in the art to incorporate the ONO layer, since it is desirable to use materials that are known and well suited for the intended use.

Response to Arguments

9. Applicant's arguments filed January 4, 2006 have been fully considered but they are not persuasive.

Applicant asserts that the 35 USC 112, second paragraph rejection of claim 14 has been overcome by the amendment to claim 14. There is no amendment in the claim related to the structure or location of the trench.

Applicant argues that Ohshima et al. do not teach a phosphorous doped oxide layer, with "said phosphorous-doped oxide layer extending no higher than the second polysilicon layer." This teaching can be seen in Fig. 5D where the phosphorus-doped oxide layer (22) extends no higher than the second polysilicon layer.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens
Examiner
Art Unit 2811